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(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 949 780 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.10.1999 Bulletin 1999/41

(51) Int Cl.[6]: **H04L 1/00**

(21) Application number: **99302748.1**

(22) Date of filing: **08.04.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **08.04.1998 JP 9585398**
15.10.1998 JP 29368898

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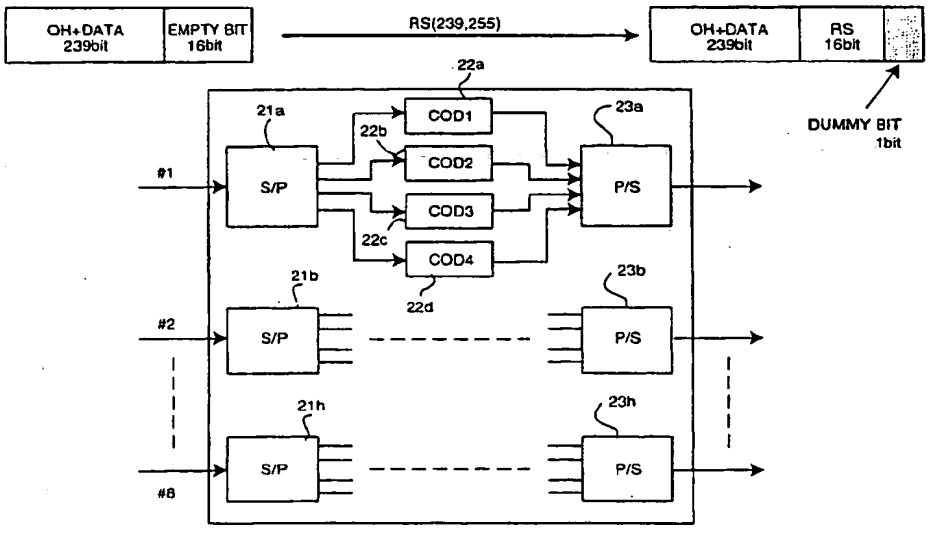
(54) A frame format and method and apparatus for processing a frame

(57) A frame format used for a codec is characterised in that, in the case in which the number of total bits used for an overhead, a data and an error correction code is B bits, and the bit number of dummy bits is D bits, the number A of total bits of one frame is A = B + D, and in the case in which the number of parallel processing inside the codec is P, the above-described bit number D of the dummy bits satisfies D P x n - B (n is a natural number).

FIG.2



EP 0 949 780 A2

Description

[0001] The present invention relates to a frame format and to a method and apparatus for processing a frame. A particular arrangement to be described by way of example in illustration of the invention is concerned with a frame format used in a Forward Error Correction section for an error correction code that is used in a main transmission apparatus.

[0002] In recent years. an increase in the amount of communication is remarkable against the background of the development of information transfer. Accordingly, the development of a high speed and large capacity transmission apparatus is urgently needed in a main transmission system. Also, at the same time as this, the small-sizing of apparatus and the reduction of cost are essential. The codec section for an error correction code used in main transmission apparatus is also no exception to this.

[0003] Accordingly, since, in an FEC (Forward Error Correction)IC that has been used conventionally, the processing speed is slow, parallel processing is conducted by means of a number of IC's for achieving high speed processing. This means that the scale of the apparatus becomes large. Accordingly, a high speed and small-sized IC is required. Actually, high speed IC, parallel processing is often conducted so as to meet the speed of an encoding section inside the IC.

[0004] A frame format has been proposed previously for use in a high speed FEC-IC, and the operation of the high speed FEC-IC will be explained, with reference to Figs. 13 to 18 of the accompanying drawings in which:-

Fig. 13 is a diagram for use in explaining a previously proposed frame format;
Fig. 14 is a block schematic diagram for use in explaining one example of a previously proposed high speed FEC-IC,
Fig. 15 is a diagram showing a bit series of one frame which is input in a previous proposal to a high speed FEC-IC,
Fig. 16 is a diagram showing the positions of bits which are processed by each COD of the high speed FEC-IC in a previous proposal,
Fig. 17 is a block schematic diagram showing a circuit arrangement of an FEC frame transformation section for use in conducting an FEC frame processing method in a previous proposal, and
Fig. 18 is an explanatory view of a data array after frame transformation in the FEC frame processing method in relation to a prior proposal.

[0005] As shown in Fig. 13, one frame is constructed of a total of 255 bits in which the first bit is an overhead (OH), 238 bits are data, and the remaining 16 bits are Reed Solomon codes (referred to as RS, hereinafter).

[0006] Now, the high speed FEC-IC for processing the data in the above-mentioned frame format will be explained.

[0007] Fig. 14 is a view for explaining one example of the high speed FEC-IC. This FEC-IC is assumed to operate with 300 MHZ so as to conduct 8 bit parallel processing (input/output #1 to #8). Also, each input of the 8 bit parallels is further divided to 4 bit parallels by means of a serial-parallel (S/P) convertor, and the speed thereof is reduced to a speed at which code processing for a correction code can be conducted. Thereafter, the Reed Solomon codes (RS) are calculated and added by each COD module, and the speed is restored to the original transmission speed by a parallel-serial (P/S) transformation.

[0008] Next, operation of the high speed FEC-IC in which a frame of the previously proposed frame format is input will be explained.

[0009] A bit series of one frame that is input to #1 of Fig. 14 is shown in Fig. 15. Each numeral in Fig. 15 shows a bit position within the frame, and it will be considered that this frame is repeatedly input.

[0010] First, a serial data of 255 bits, which has been input from #1, is transformed to a 4 bit parallel data by the S/P transformation. Encoding of RS on the data is conducted by COD1 to COD4, respectively, and thereafter, the speed is restored to the original speed by the P/S transformation.

[0011] A bit series that is processed by the COD1 to COD4 at this time is shown in Fig. 16. Since the serial data of 255 bits is processed by the 4 bit parallels, the bit positions at which each COD conducts the processing are different for each frame (shifted by one bit).

[0012] By the way, in order to resolve the above-mentioned shift of the bit positions at which each COD conducts the processing by means of a hardware, it is necessary to incorporate a buffer in the IC or to add a function capable of accommodating itself to the shift in the COD modules.

[0013] However, if such a means is arranged, the arrangement results in a lowering of a processing speed or large-sizing of the IC.

[0014] Next, operation of the receiving the FEC frame be explained. In a previously proposed FEC frame processing, an optical signal of 32,640 bits that has been input is divided into 128. Since this optical signal is processed by the even-number of circuits, the circuit size of an FEC frame transformation section becomes large, and the processing is inefficient.

[0015] Fig. 17 simply shows an arrangement of the FEC frame transformation section in relation to the prior proposals, and shows here that four parallel processing is applied to the even-number of the 255 bits optical signal transformed in a serial-parallel convertor 170.

[0016] The first bit is removed out of the respective optical signals to which the four parallel processing was applied in this manner, since it is an OH signal, and then, 239 - 255 bits of Reed Solomon signals (syndromes) are removed. This situation is shown in Fig.18. An upper column to a lower column in the table show contents to be

processed in each of frame transformation sections 171-174. It is shown that numbers with half-tone in this table are to be removed, respectively.

[0017] Features of a frame format, frame processing and apparatus to be described below, by way of example in illustration of the invention are that the hardware arrangement within the FEC-IC becomes comparatively simple, and high speed processing and small-sizing can be achieved and that a frame format for accomplishing the above-described features can be obtained with high compatibility with the conventional system.

[0018] In a particular arrangement to be described below by way of example in illustration of the present invention a frame format is used for a codec, in which, where the number of total bits used for an overhead, a data and an error correction code is B bits, and the bit number of dummy bits is D bits, the number A of total bits of one frame is

$A = B + D$, and where the number of parallel processing inside the codec is P, the above-described bit number D of the dummy bits satisfies $D = P \times n - B$ (n is a natural number).

[0019] In addition, for the above-described error correction code, a Reed Solomon code is used as a typical example.

[0020] Also, it is possible to use the above-described dummy bits as an arbitrary information bit.

[0021] One particular arrangement to be described below by way of example in illustration of the present invention includes a frame processing method of a codec in which the number of parallel processing is P, and in which when processing a bit series in which the number of total bits of one frame is A bits, each parallel processing section adds dummy bits in addition to an error correction code, and thereby, the process is conducted so that bit positions of the bit series which are processed by each parallel processing section are not different for every frame.

[0022] In addition, in the case in which the number of total bits used for an overhead, a data and an error correction code is B bits, and the number of parallel processing of the codec is P. the bit number D of the above-described dummy bits is $D = P \times n - B$ (n is a natural number).

[0023] Also, if the above-described dummy bits are processed as an arbitrary information bit, it is possible to incorporate information into the dummy bits.

[0024] In the frame format for the codec to be described below as an example in illustration of the present invention, the dummy bits are added to a frame arrangement that has been used conventionally, in accordance with the number of parallel processing operations inside the codec.

[0025] The above-described features are obtained by one exemplary FEC frame processing method in which an FEC frame included in an optical signal to be input is divided into one hundred twenty eight, and the optical signal divided into one hundred twenty eight is processed by means of a three parallel method in applying serial-parallel converting to the optical signal, and by an FEC frame processing method in which an optical signal to which serial/parallel converting is applied in accordance with a three parallel method is output as an optical signal forming an FEC frame by means of multiplexing of one hundred twenty eight.

[0026] There will also be described an exemplary FEC frame processing apparatus which has a serial/parallel convertor for converting an FEC frame of a serial system, which is divided into one hundred twenty eight, into three parallels, and bit removal means for removing a bit at a previously fixed bit position of each signal that was converted.

[0027] In a FEC frame processing method to be described as an example in illustration of the present invention, after an FEC frame included in an optical signal to be input and output is divided into 128, the optical signal divided into one hundred twenty eight is processed by means of the three parallel method. According to such three parallel processing, the removal of the OH signal and the Reed Solomon signals can be easily conducted, and the scale of the hardware circuit to be mounted for processing the FEC frame is reduced. In other words, as a result of adopting the three parallel method, since a frame pattern that is processed in each frame transformation becomes to be one pattern, the processing is simplified, and it is possible to reduce the scale of the hardware circuit to be mounted.

[0028] The following description and drawings disclose, by means of examples, the invention which is characterised in the appended claims, whose terms determine the extent of the protection conferred hereby.

[0029] In the drawings:-

Fig. 1 is a view showing one example of a frame format for a high speed FEC-IC,

Fig. 2 is a block diagram showing one example of the high speed FEC-IC,

Fig. 3 is a view showing an example of a serial data which is input to the high speed FEC-IC shown in Fig. 2,

Fig. 4 is a view showing positions of bits which are processed by each COD of the high speed FEC-IC shown in Fig. 2,

Fig. 5 is a block diagram showing a generalized high speed FEC-IC,

Fig. 6 is a view for explaining a generalized frame format,

Fig. 7 is a block diagram showing an embodiment of a circuit arrangement appropriate for conducting an FEC frame processing method (reception),

Fig. 8 is a block diagram showing an embodiment of an FEC frame transformation section appropriate for conducting the FEC frame processing method,

Fig. 9 is an explanation view of an FEC frame of an optical signal to be processed,

Fig. 10 is an explanation view of a frame format after

serial/parallel converting,

Fig. 11 is an explanation view of a data array after a frame transformation, and

Fig. 12 is a block diagram showing an embodiment of a circuit arrangement appropriate for conducting an FEC frame processing method (transmission).

[0030] First, one example of a frame format for a high speed FEC-IC will be explained. Fig. 1 is a view showing one example of a frame format for a high speed FEC-IC.

[0031] In the conventional frame format, one frame is constructed of a total of 255 bits in which the first one bit is an overhead (OH), 238 bits are data, and the remaining 16 bits are Reed Solomon codes.

[0032] However, in the frame format for the high speed FEC-IC to be described in illustration of the present invention, in addition to the conventional frame format, by taking into account that 4 bit parallel processing is applied to inputs in the IC, 256 bits are realized by adding a dummy bit of 1 bit.

[0033] Now, a high speed FEC-IC to which the frame format for the high speed FEC-IC is input will be described. Fig. 2 is a block diagram showing one example of the high-speed FEC-IC.

[0034] This high speed FEC-IC operates at 300 MHZ so as to conduct 8 bit parallel processing (input/output #1 to #8).

[0035] Also, each input (#1 to #8) of the 8 bit parallels is further divided to 4 bit parallels by means of serial-parallel (S/P) convertors 21a - 21h, and the speed is reduced to a speed at which code processing for a correction code can be conducted.

[0036] In each of COD modules 22a - 22d, Reed Solomon codes are calculated and added, and a dummy bit of 1 bit is added.

[0037] Data output from each of the COD modules 22a - 22d are input to parallel-serial (P/S) transformations 23a - 23h, and the speed is restored to the original transmission speed.

[0038] Next, the operation of this embodiment will be explained. In order to make the explanation easy to understand, the operation will be explained by focusing on an input #1 in Fig. 2. Actually, the operation explained below is processed from #1 to #8 in parallel.

[0039] First, a serial data of 256 bits as shown in Fig. 3 is input to the input #1. Then, this serial data of 256 bits is transformed to a 4 bit parallel data by means of the S/P transformation 21a. Bit series which are processed by each of the COD 22a to the COD 22d at this time are shown in Fig. 4.

[0040] Since the dummy bit is being added to by 1 bit, 256 can be divided by 4 and the positions of the bits which are processed by each of the COD 22a to 22d do not change for every frame, and a task such as a bit shift which occurs in the above-mentioned conventional frame arrangement can be avoided. In addition, 0 or 1 which does not have a specific meaning can be allocated to the dummy bit, and some information can be allocated, however. In the above-mentioned example, even though 1 + 4 x N bits (N is a natural number) are allocated to the dummy bit, much information can be put on without causing a shift of the bit positions. Management information ofa transmission system and so forth can be the information to be put on.

[0041] Although, in the above-mentioned example, an example of one bit as the dummy bit was explained, a case in which the frame format is generalized will be explained.

[0042] An FEC-IC to which a bit series is input is shown in Fig. 5. In Fig. 5, the FEC-IC is shown, in which the number of processing in the FEC-IC is K, and the number of parallel processing of each processing is P.

[0043] Here, assuming that the number of parallel processing steps inside the FEC-IC is P, the number of bits of the conventional frame format is B, and the number of bits of the dummy bit is D, a proposed frame format can be represented as shown in Fig. 6. However, the bit number D of the dummy bit must satisfy the following equation:

$$B + D = P \times N \text{ (N is a natural number)} \quad (1)$$

[0044] For example, if in the above-mentioned example P = 4 and B = 255, and if these values are assigned into the equation (1),

$$255 + D = 4 \times N \quad (2)$$

[0045] Since D is a positive integer $N \geqq 64$ and if a case of N = 64 is considered,

$$255 + D = 256 \quad (3)$$

and accordingly, D can be set: D = 1 bit.

[0046] Also, in the case in which it is desired that much information is put on the dummy bit, N is set: N = 65, for example,

$$255 + D = 260 \quad (4)$$

and accordingly, D can be set: D = 5 bits.

[0047] By using the frame format described in a type of the high speed FEC-IC in which the speed is reduced by means of the S/P transformation inside the IC, compared with the case in which the conventional frame arrangement is employed, the number of buffers in the FEC-IC becomes less, the hardware arrangement becomes more simple, and a high speed and small-sizing of the IC can be realized.

[0048] Also, since a format equivalent to the previously proposed format can be obtained by removing only a dummy bit by means of a dummy bit removing circuit, a

high degree of compatibility with the previously proposed conventional system is possible.

[0049] Next, frame processing illustrative of the present invention will be described. Referring to Fig. 7 showing an arrangement of a first embodiment, in an optical signal receiving section 71, an optical signal formed of an FEC frame is received, and the optical signal formed of the FEC frame is divided into eight.

[0050] In a first FEC frame decode section 72, each signal that was divided into eight is divided by two and into sixteen signals. In a second FEC frame decode section 73, the optical signals that were previously divided by two are further divided by eight and into one hundred twenty eight signals.

[0051] A serial-parallel convertor 74 at the next stage is an assembly of individual serial-parallel convertors 74a-74c arranged correspondingly to the respective signals. The individual serial-parallel convertors 74a-74c apply serial-parallel converting to the signals that were divided into one hundred twenty eight through the above-mentioned process, and provide the signals to three respective FEC frame transformation sections 81 - 83 that are arranged as shown in Fig. 8. An FEC frame transformation section 75 of Fig. 7 is formed by three such FEC frame transformation sections 84-83.

[0052] Out of the respective optical signals that were divided into three in the FEC frame transformation section 75. as mentioned below with reference to Fig. 9, an OH signal and Reed Solomon signals of the FEC frame are removed.

[0053] Fig. 9 shows the FEC frame of an optical signal that is input to the optical signal receiving section 71, in which the FEC frame is constructed of a format of a total of 32,640 bits, which is formed of an OH signal of 128 bits, information signals of 30,464 (= 238 x 128) bits, and RS signals of 2,048 (= 16 x 128) bits.

[0054] If the optical signal of Fig. 9 is divided into one hundred twenty eight in a manner as mentioned in connection with Fig. 7, when the optical signals are input to the serial-parallel convertor 74, the FEC frame of Fig. 9 comes to have a frame format of a total of 255 bits consisting of an OH signal of 1 bit, information signals of 238 bits and RS signals of 16 bits, as shown in Fig. 10. The signals that were divided into one hundred twenty eight are separated into three signals and processed through the serial-parallel convertor 74.

[0055] In the FEC frame transformation sections 81 - 83 of Fig. 8, by removing bits, which are always fixed, such as 1 (= an OH signal) and 239-255 (=RS signals) that correspond to half-tone parts shown in Fig. 11. it is possible to remove the OH signal and the Reed Solomon signals (syndromes) that are included the optical signal.

[0056] With regard to the effect of the presently proposed arrangement, conventionally, the signals are divided into four and are processed by means of the serial-parallel convertor 170 shown in Fig. 17. However, in the case in which the signals are divided into four, since as shown in Fig. 18 there are four patterns of the OH signal and the Reed Solomon signals to be removed, the scale of the circuit on which the frame transformation sections 171-174 of Fig. 17 are mounted becomes large. To the contrary, in the present arrangement, by dividing the signals into three as shown in Fig. 8, it becomes possible to reduce the scale of the circuit hardware.

[0057] Although Fig. 7 and Fig. 8 are embodiments showing the processing for the signals that are input (received), similarly the same concept can be used for signals that are output (transmitted). Fig. 12 shows this arrangement, and although it is almost the same arrangement as Fig. 7, signals go forward in the opposite direction. In an FEC frame transformation section 121, the three parallel method is applied for processing a data that is formatted as shown in Fig. 11. After that, the data is transformed into serial signals in the serial-parallel convertors 122.

[0058] The signals obtained that were divided into one hundred twenty eight are encoded into sixteen signals in a first FEC frame encode section 123. and then, the signals are encoded into eight signals in a second FEC frame encode section 124, and then, an optical signal is output (transmitted) through an optical signal transmitting section 125.

[0059] In the processing during such an output also, the arrangement operates in a similar way to the case of the input, and by dividing the signals into three and processing them, the removal of unnecessary signals can be conducted by means of a simple circuit arrangement, and it is possible to reduce the scale of the circuit hardware to be provided.

[0060] It will be understood that although particular arrangements have been described, by way of example in illustration of the present invention, variations and modifications thereof, as well as other arrangements, may be conceived within the scope of the appended claims.

Claims

1. A frame format used for a codec in which where the number of total bits used for an overhead, a data and an error correction code is B bits, and the bit number of dummy bits is D bits, the number A of total bits of one frame is

$$A = B + D,$$

and where the number of parallel processing inside the codec is P, the bit number D of the dummy bits satisfies

$$D = P \times n - B$$

(n is a natural number).

2. A frame format used for a codec as claimed in claim 1, wherein the error correction code is a Reed Solomon code.

3. A frame format used for a codec as claimed in claim 1, wherein the dummy bits are used as an arbitrary information bit.

4. A frame processing method of a codec in which the number of parallel processing is P, including the steps of

processing a bit series in which the number of total bits of one frame is A bits, each parallel processing section adding dummy bits in addition to an error correction code and
processing so that bit positions of the bit series which are processed by each parallel processing section are not different for every frame.

5. A frame processing method of a codec as claimed in claim 4, wherein in the case in which the number of total bits used for an overhead, a data and an error correction code is B bits, and the number of parallel processing of the codec is P, the bit number D of the dummy bits is

$$D = P \times n - B$$

(n is a natural number).

6. A frame processing method of a codec as claimed in claim 4, wherein the dummy bits are processed as an arbitrary information bit.

7. An FEC frame processing method including the step of dividing an FEC frame into one hundred twenty eight and processing the signal divided into one hundred twenty eight by means of a three parallel method employing serial/parallel converting.

8. A FEC frame processing method as claimed in claim 8, wherein the signal divided into one hundred twenty eight is a frame format of a total of 255 bits.

9. An FEC frame processing method including the steps of converting a parallel signal to a serial signal by means of a three parallel method, and multiplexing the serial signal by one hundred and twenty eight.

10. An FEC frame processing apparatus including a serial/parallel convector for converting an FEC frame of a serial system, which is divided into one hundred twenty eight. into three parallel sections and bit removal means for removing a bit at a previously fixed bit position of each signal that was converted.

FIG.1

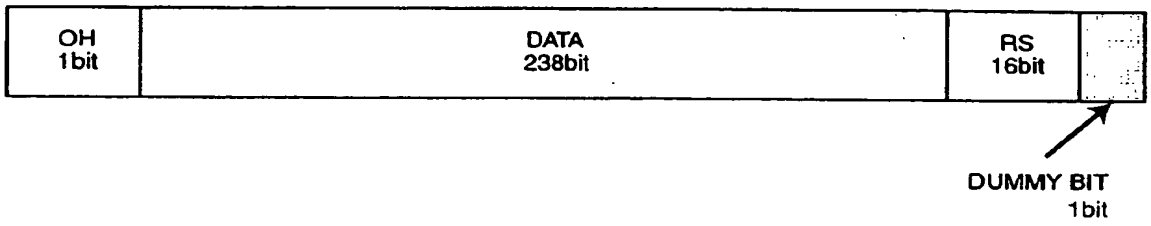


FIG.2

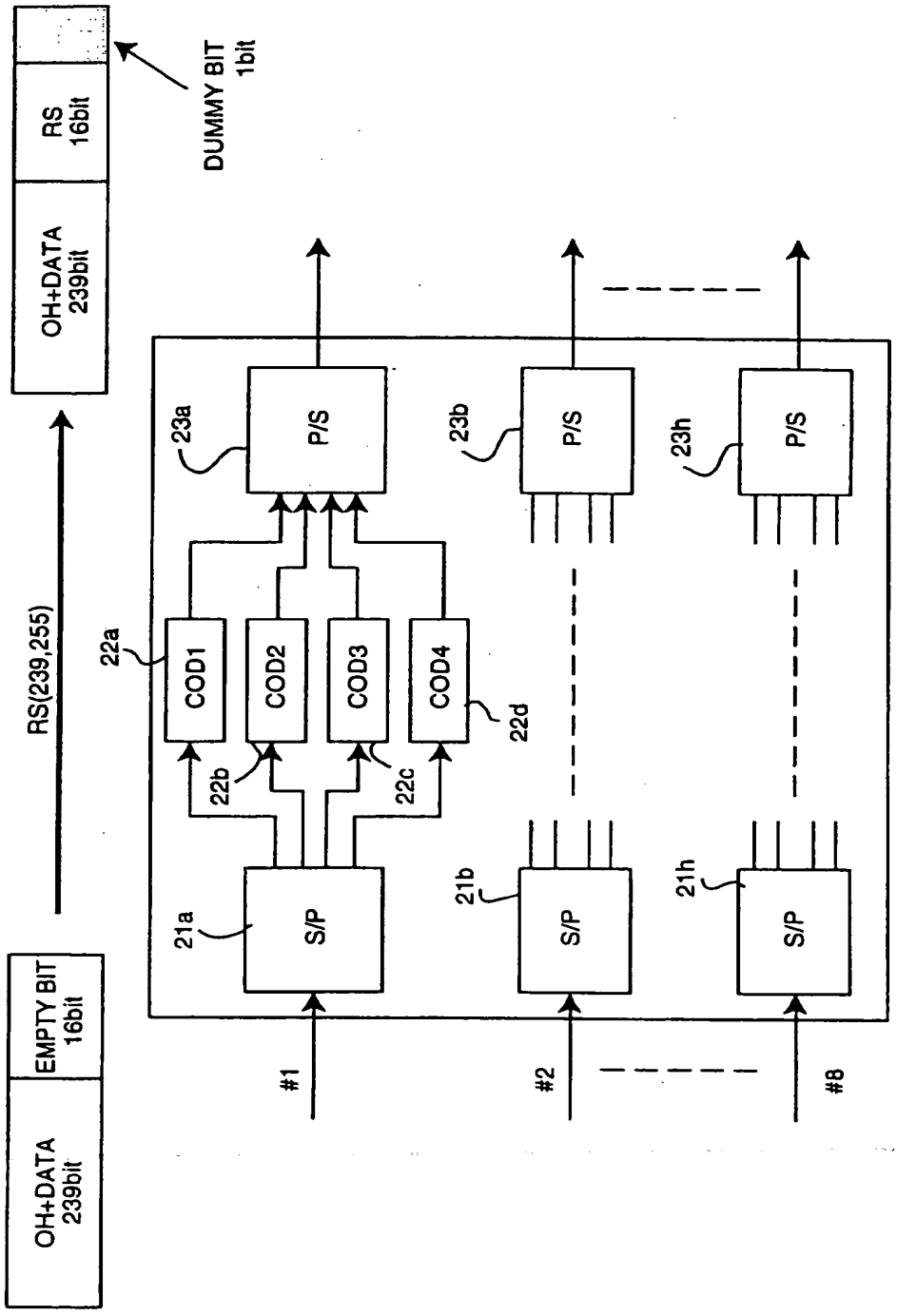

OH+DATA 239bit
EMPTY BIT 16bit
RS(239,255)
OH+DATA 239bit
RS 16bit
DUMMY BIT 1bit
21a
S/P
21b
S/P
21h
S/P
22a
COD1
COD2
COD3
COD4
22b
22c
22d
23a
P/S
23b
P/S
23h
P/S
#1
#2
#8

FIG.3

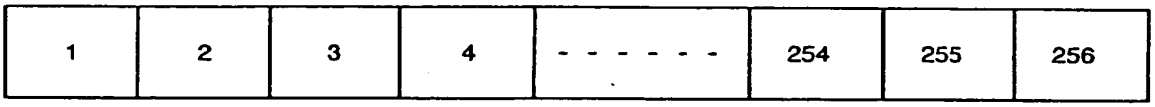


FIG.4

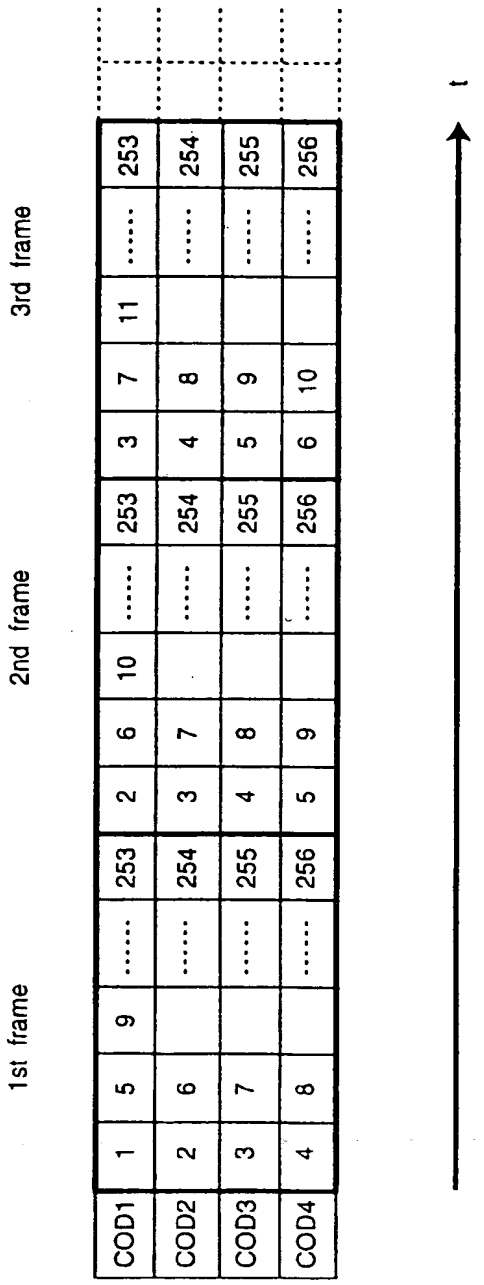

1st frame
2nd frame
3rd frame
COD1
COD2
COD3
COD4
1
2
3
4
5
6
7
8
9
10
11
253
254
255
256
t

FIG.5

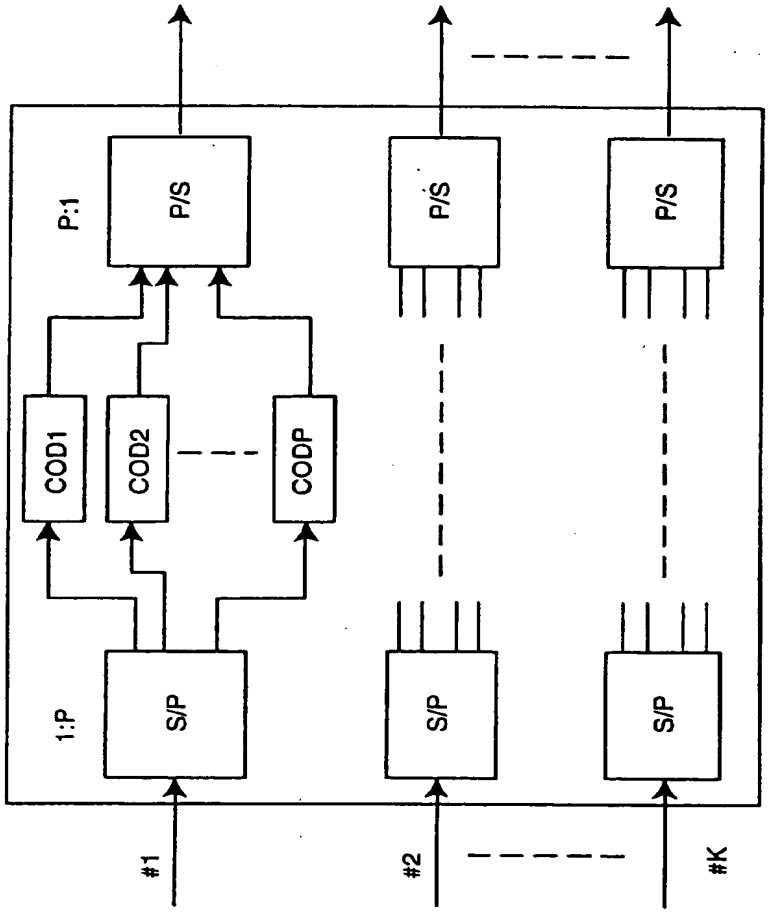

P:1
P/S
P/S
P/S
COD1
COD2
CODP
1:P
S/P
S/P
S/P
#1
#2
#K

FIG.6

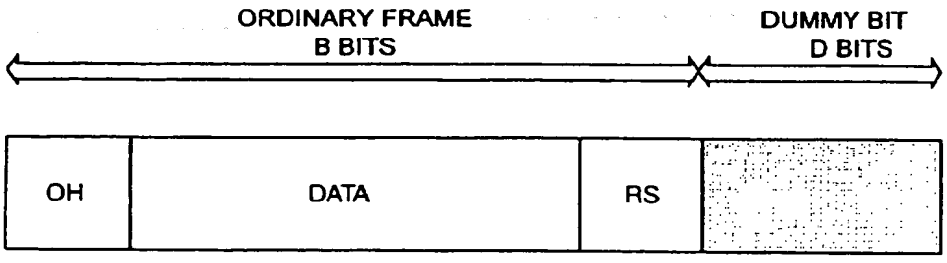

ORDINARY FRAME
B BITS
DUMMY BIT
D BITS
OH
DATA
RS

FIG.7

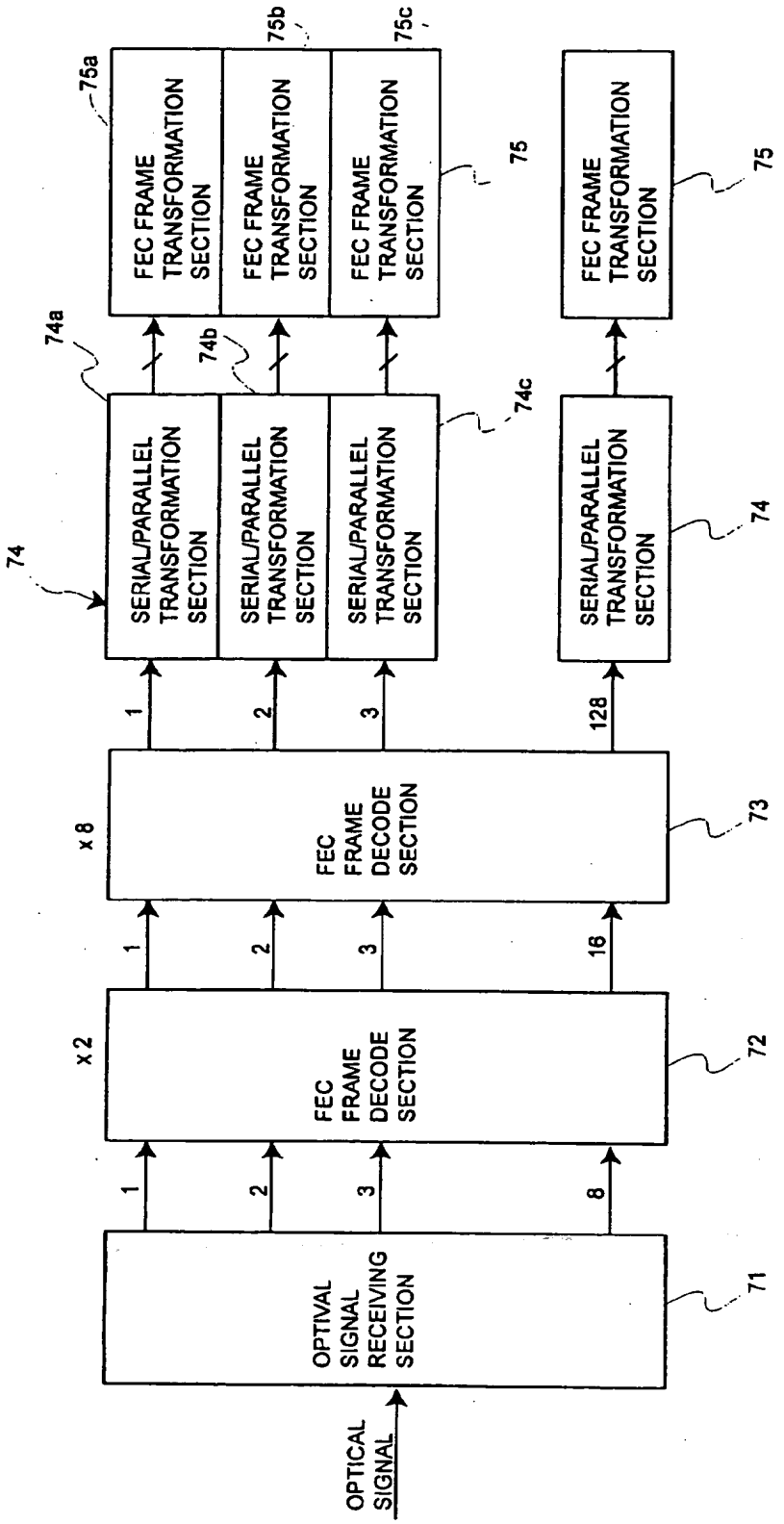

OPTICAL SIGNAL
OPTIVAL SIGNAL RECEIVING SECTION
71
1
2
3
8
x 2
FEC FRAME DECODE SECTION
72
1
2
3
16
x 8
FEC FRAME DECODE SECTION
73
1
2
3
128
74
74a
74b
74c
SERIAL/PARALLEL TRANSFORMATION SECTION
SERIAL/PARALLEL TRANSFORMATION SECTION
SERIAL/PARALLEL TRANSFORMATION SECTION
SERIAL/PARALLEL TRANSFORMATION SECTION
75
75a
75b
75c
FEC FRAME TRANSFORMATION SECTION
FEC FRAME TRANSFORMATION SECTION
FEC FRAME TRANSFORMATION SECTION
FEC FRAME TRANSFORMATION SECTION

FIG.8

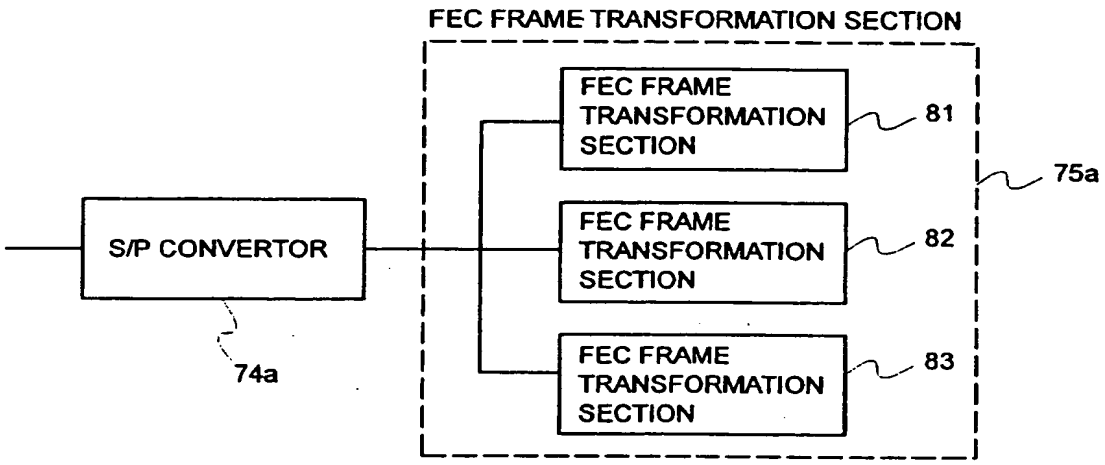

FEC FRAME TRANSFORMATION SECTION
FEC FRAME TRANSFORMATION SECTION
81
75a
S/P CONVERTOR
FEC FRAME TRANSFORMATION SECTION
82
74a
FEC FRAME TRANSFORMATION SECTION
83

FIG.9

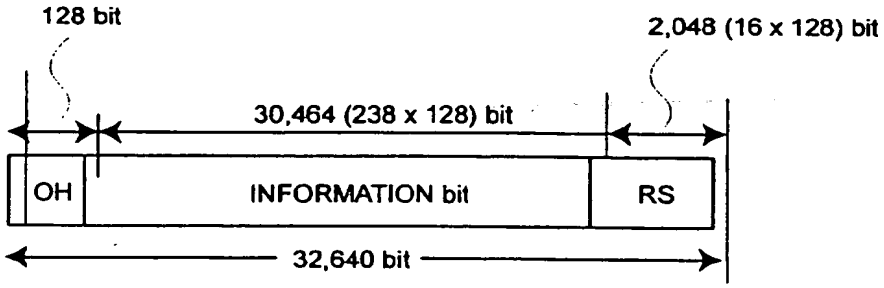

128 bit
2,048 (16 x 128) bit
30,464 (238 x 128) bit
OH
INFORMATION bit
RS
32,640 bit

FIG.10

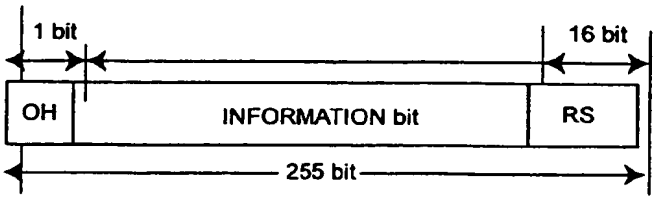

1 bit
16 bit
OH
INFORMATION bit
RS
255 bit

FIG.11

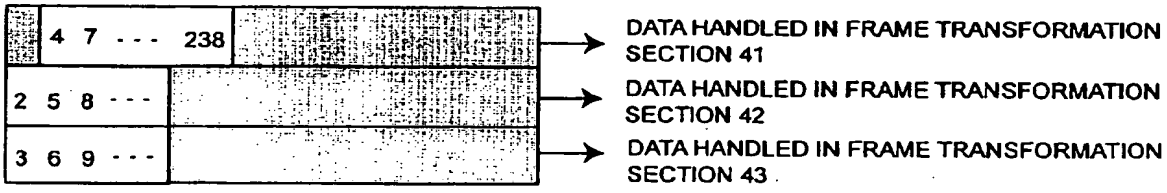

4 7 - - - 238
2 5 8 - - -
3 6 9 - - -
DATA HANDLED IN FRAME TRANSFORMATION SECTION 41
DATA HANDLED IN FRAME TRANSFORMATION SECTION 42
DATA HANDLED IN FRAME TRANSFORMATION SECTION 43

FIG.12

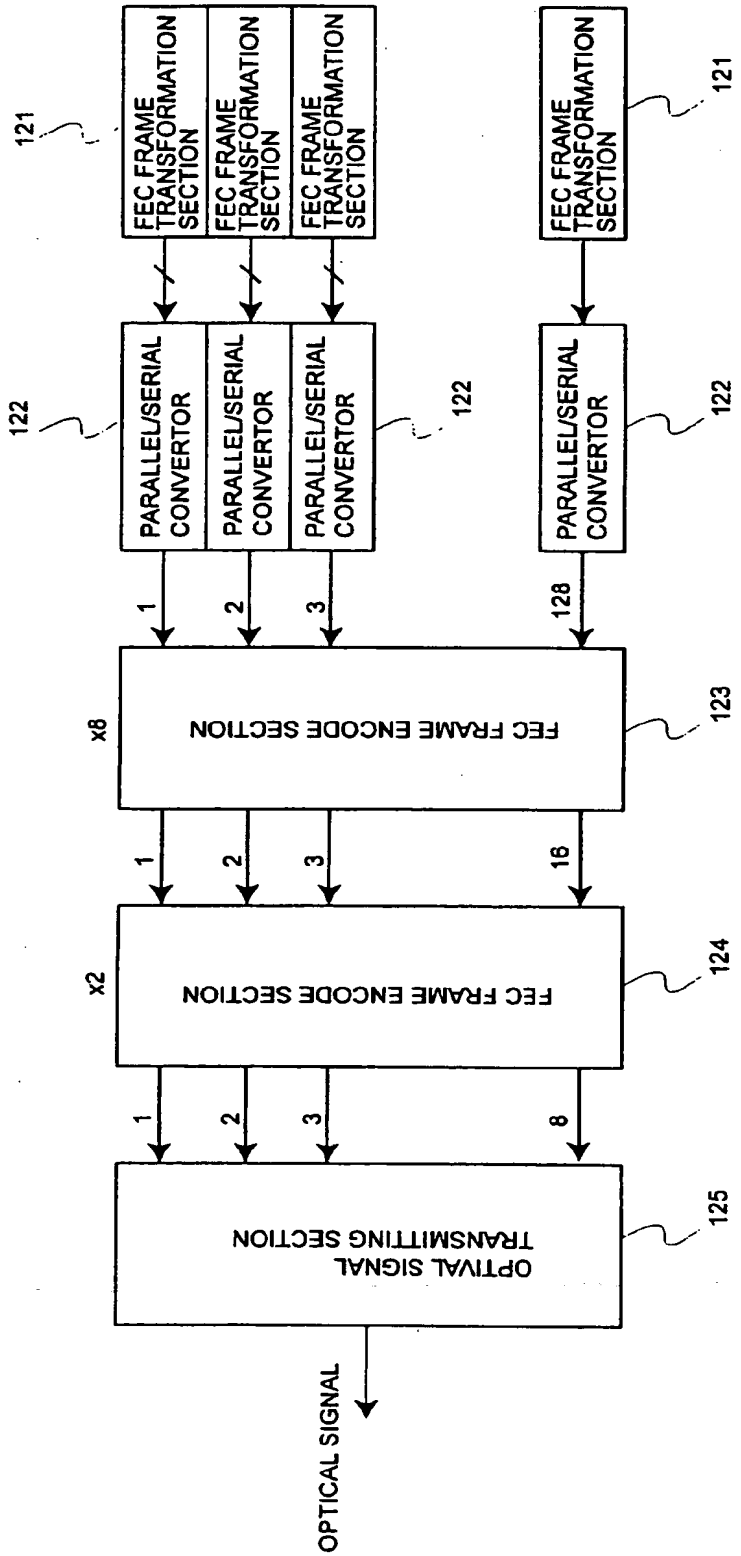

FEC FRAME TRANSFORMATION SECTION
FEC FRAME TRANSFORMATION SECTION
FEC FRAME TRANSFORMATION SECTION
FEC FRAME TRANSFORMATION SECTION
121
121
PARALLEL/SERIAL CONVERTOR
PARALLEL/SERIAL CONVERTOR
PARALLEL/SERIAL CONVERTOR
PARALLEL/SERIAL CONVERTOR
122
122
122
1
2
3
128
x8
FEC FRAME ENCODE SECTION
123
1
2
3
16
x2
FEC FRAME ENCODE SECTION
124
1
2
3
8
OPTIVAL SIGNAL TRANSMITTING SECTION
125
OPTICAL SIGNAL

FIG.13

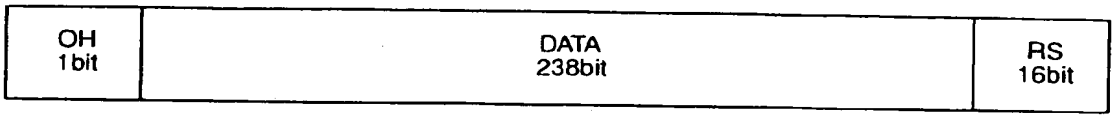


FIG.14

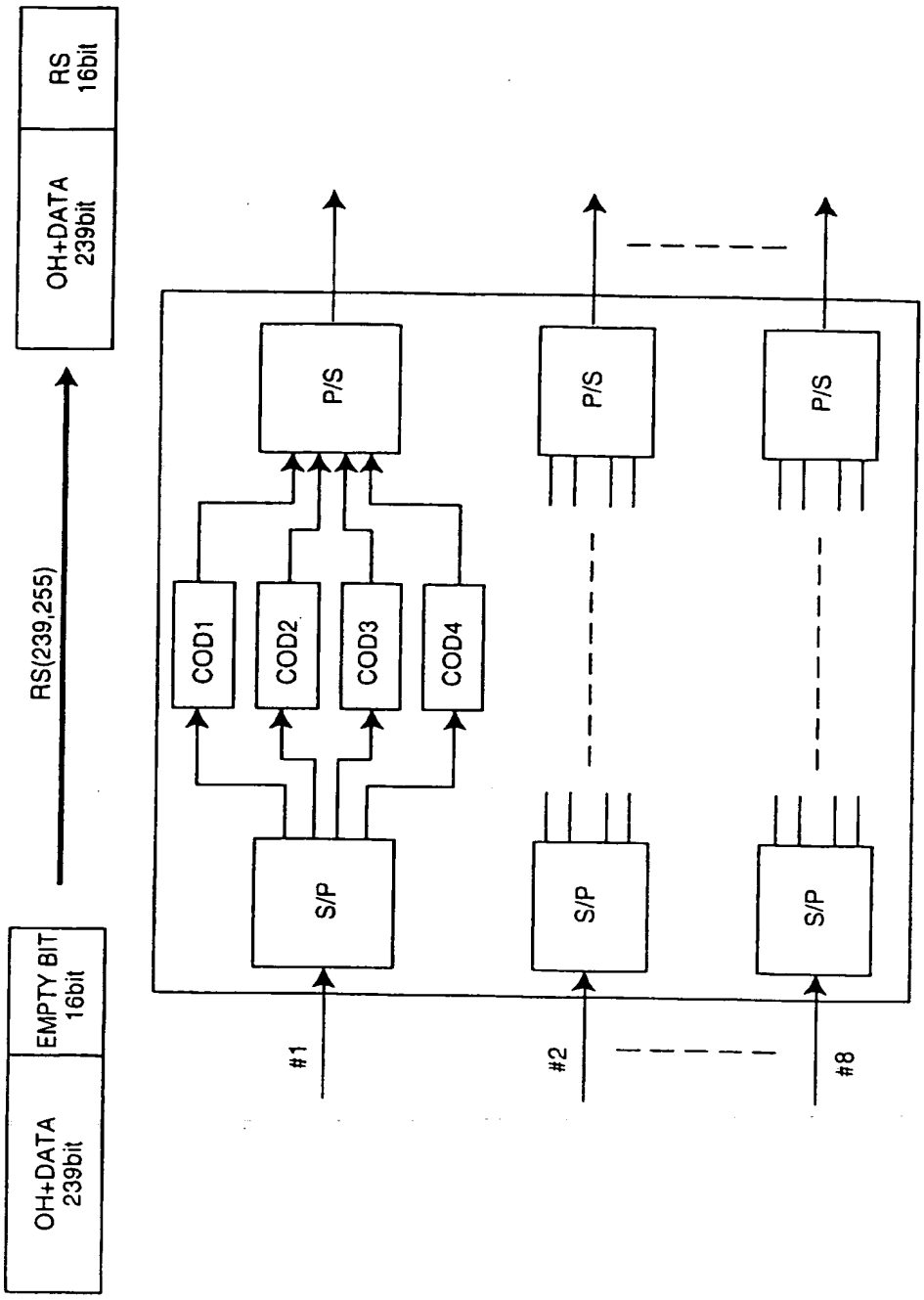

OH+DATA 239bit
EMPTY BIT 16bit
RS(239,255)
OH+DATA 239bit
RS 16bit
COD1
COD2
COD3
COD4
S/P
S/P
S/P
P/S
P/S
P/S
#1
#2
#8

FIG.15

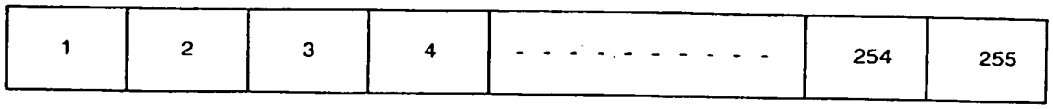


FIG.16

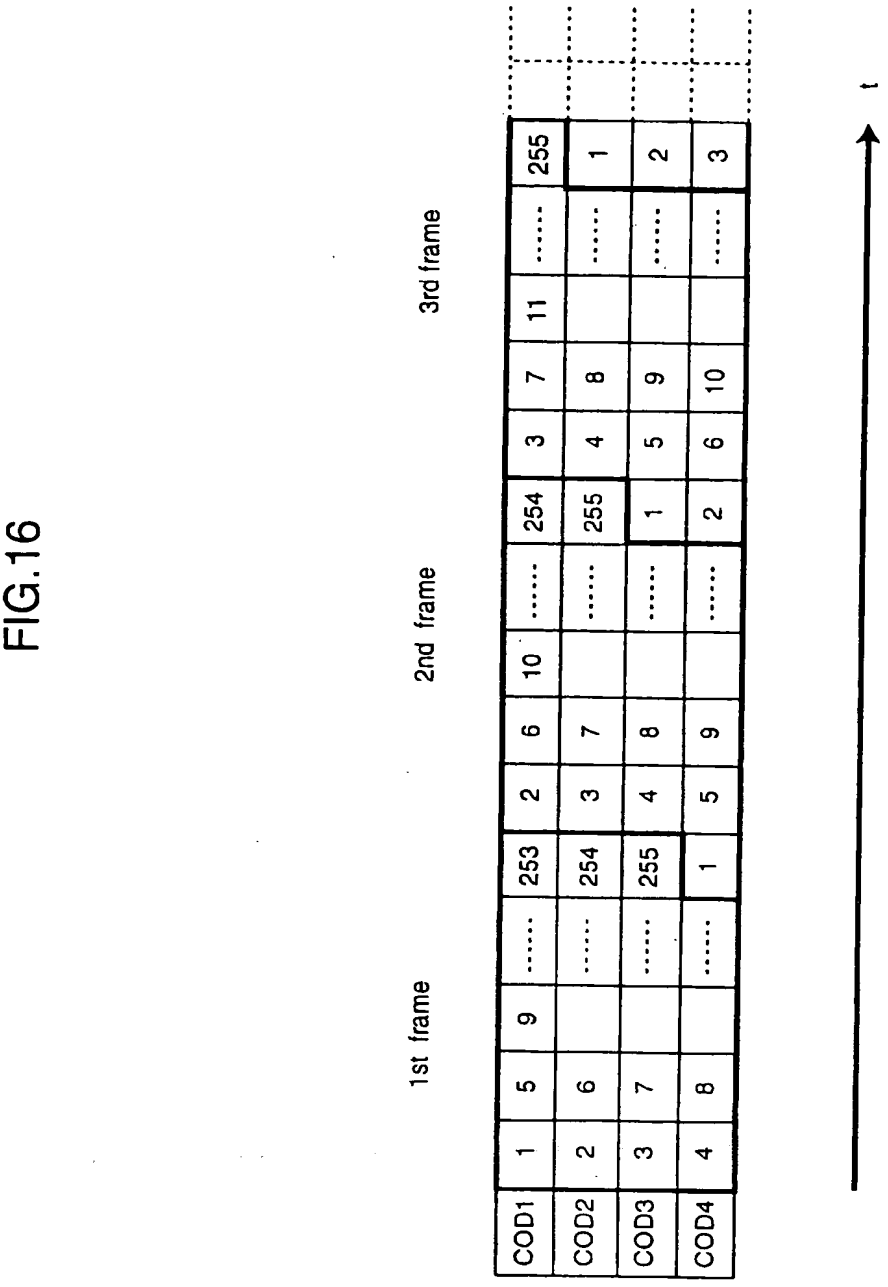

1st frame
2nd frame
3rd frame
t
COD1
COD2
COD3
COD4
1
2
3
4
5
6
7
8
9
10
11
253
254
255
1
2
3
4
5
6
7
8
9
10
254
255
1
2
3
4
5
6
7
8
9
10
11
255
1
2
3

FIG.17

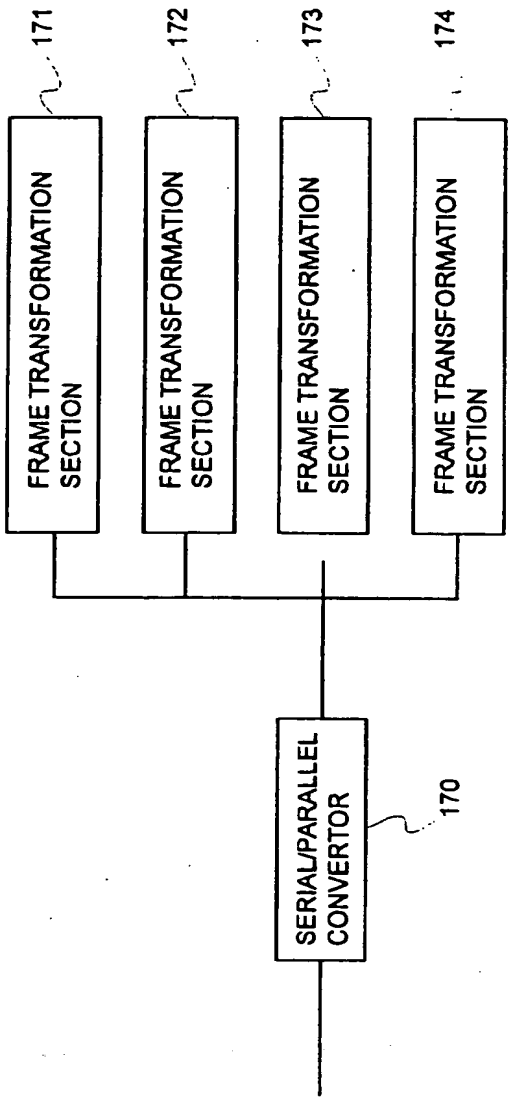
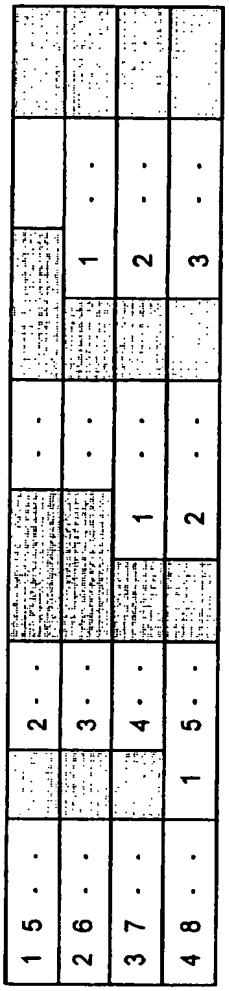

171
172
173
174
FRAME TRANSFORMATION SECTION
FRAME TRANSFORMATION SECTION
FRAME TRANSFORMATION SECTION
FRAME TRANSFORMATION SECTION
SERIAL/PARALLEL CONVERTOR
170

FIG.18



* DATA IN THE ORDER SHOWN FROM UPPER COLUMN ARE HANDLED IN FRAME TRANSFORMATION SECTIONS 51 - 54.
* 1: BE REMOVED DUE TO OH
* 239 - 255: BE REMOVED DUE TO RS